REMARKS

These remarks are in reply to the Office Action mailed December 29, 2005. Claims 1-42 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Pat. to Wollan et al.[1] ("Wollan"). Applicant respectively disagrees with the rejections.

The Wollan Reference

Wollan discloses an "eight bit data bus 12," a RAM, and an "REGISTER FILE 20" that is "separate from the RAM." According to Wollan,

> "an indirect-address bus 14 provides indirect addressing. The indirect-address bus 14 includes a means for receiving an address from the REGISTER FILE, namely the bus interface 14' which couples the REGISTER FILE to the indirect-address bus 14 for transmitting an address either to the RAM or to a PROGRAM COUNTER 28."[2]

According to Figure 1 of Wollan, and in contrast to the Wollan eight bit data bus 12, the "indirect-address" bus 14 is sixteen bits wide. Wollan explains that:

> "the REGISTER FILE . . . includes register circuitry 100 which provides thirty-two eight bit registers R0-R31 . . . the register circuitry 100 is capable of provisioning the last six registers R26-R31 as three pairs of logical sixteen bit registers . . . (X), . . . (Y), . . . (Z). A common bus interface consisting of two sixteen-line data buses 102, 104 provide respectively a data-in and a data-out bus for the sixteen bit registers.
>
> * * *
>
> The sixteen bit registers provided by the REGISTER FILE are used as indirect address register pointers for RAM and program-space addressing."[3]

Wollan also discloses "selector control circuitry 134" and control lines "R_SEL and WE_R," further stating that:

> "the bank of eight flip-flops corresponding to each register R0-R31 is written to by presenting input to the D leads and by asserting the clock lines CK of the flip-flops . . . *the selector control circuitry 134 . . . asserts the proper CK signals so that the correct register*

[1] No. 5,809,327
[2] Wollan, col. 4, lines 22-27.
[3] Wollan, col. 4, line 62 to col. 5, line 13.

> *and bit(s) are written.* The R_SEL and WE_R control lines cooperate to write the eight flip-flops corresponding to a selected register. The WE_XH, WE_XL, WE_YH, WE_YL, WE_ZH, and WE_ZL control lines enable a write to the sixteen bit X, Y, and Z registers."[4] (emphasis added.)

To restate the emphasized language: the Wollan selector control circuitry 134 asserts various signals so that data is written to the correct register.

Moreover, the two sixteen-line data buses 102, 104 disclosed in Wollan, which provide respectively a data-in and a data-out bus for the sixteen bit registers, are coupled with the 16-bit bus 14. Thus, the "indirect-address" bus 14 does not disclose the addressing of a memory space having 2^M addresses using an N-bit bus, where M is greater than N.

Claims 1 and 23

Although the Examiner says that the Wollan reference includes a step of:

> "(d) addressing one of said two registers according to the incremented count in step (c)"[5]

and a step of

> "(c) addressing one of the at least two registers according to the incremented count in step (b)"[6]

the Wollan reference fails to disclose such steps. As explained below, Wollan discloses a method for addressing registers which is different from that claimed. Wollan discloses that registers are addressed using the five bit control line R-SEL.

The Wollan selector control circuitry 134 includes a decoder unit 140. "The decoder unit 140 is a 1:32 decoder which asserts any one of the 32 output in response to decoding R_SEL. Each output line of the decoder corresponds to a register."[7] Wollan states:

> "Consider, for example, the writing of data into register R0. The five bit control line R_SEL is set to select register R0. The

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[4] Wollan, col. 6, lines 29-44.
[5] Claim 1.
[6] Claim 23.
[7] Wollan, col. 7, lines 6-9.

> decoder 140 decodes the line, thereby asserting the output line corresponding to register R0."[8]

Thus, the Wollan decoder 140 is employed to decode the five bit control line R_SEL. Wollan nowhere discloses "(d) addressing one of said two registers according to the incremented count in step (c)." Nor does the reference disclose "(c) addressing one of the at least two registers according to the incremented count in step (b)." Accordingly, the Wollan reference fails to disclose each and every element of independent claims 1 and 23.

Claims 1 and 23

Claims 2-11 depend from claim 1. Claims 24-33 depend from claim 23. Claims 2-11 and 24-33 are not anticipated for the same reason that the independent claims 1 and 23 are not anticipated.

Claim 12

According to the Office Action, the Wollan reference includes:

> "a logic circuit adapted for:
>
> * * *
>
> (iii) addressing one of said two registers according to the incremented count in step (ii)"

The Wollan reference, however, fails to disclose such a circuit.

As explained above, Wollan discloses that registers are addressed using the five bit control line R-SEL. Further, the Wollan decoder 140 is employed to decode the five bit control line R_SEL. The Wollan reference fails to disclose that registers are addressed "according to the incremented count." Accordingly, the Wollan reference fails to disclose each and every element of independent claim 12.

Claims 13-22

Claims 13-22 depend from claim 12. Claims 13-22 are not anticipated for the same reason that the independent claim 12 is not anticipated.

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[8] Wollan, col. 7, lines 52-54.

Claim 37

Amended claim 37 includes:

> "(b) a logic circuit adapted for receiving a memory access command that does not specify said registers, and accessing the memory space at said address as a result of said memory access command."

The Wollan reference fails to disclose such a circuit.

In the rejection of claim 37, the Examiner cites col. 14, lines 46-65 of the Wollan reference. The cited text describes two instructions "for transferring data to a specified register from a memory location addressed by an X, Y, Z register; and . . . for transferring data from a specified register to a memory location addressed by an X, Y, Z register." The cited text explains that these instructions require two clock cycles to execute:

> "during the first clock cycle . . . control lines *select the register pair* of the desired sixteen-bit register . . . The ADDR_SEL control line operates selector 114 to place the B:A outputs onto the indirect address bus 14 . . . During the second clock cycle, the memory is strobed either to load data from memory onto the bus 12 (LD) or to write data into memory (ST)."[9] (emphasis added.)

Thus, Wollan teaches a data transfer instruction that includes selecting a register pair. Accordingly, Wollan fails to teach a memory access command that does not specify the claimed at least two registers. Therefore, the Wollan reference fails to disclose each and every element of independent claim 37.

In connection with claim 37, Applicant notes that the specification of the present application provides:

> "It will be recalled that in the prior art, a memory access requires an operation in which the address of the data port is placed on the data bus, as shown in Figures 3-4 as address cycles 3, 3'. In contrast, the memory devices 51, 56, and 60, according to the invention, are adapted to perform a memory access without the need to first perform the operation represented by the address cycle 3 and 3' in

[9] Wollan, col. 14, lines 46-65

> Figures 3-4. According to the invention, a memory access may occur immediately subsequent to the storage of a complete address for a location L in the registers R1-RK. In other words, once a memory location L has been addressed, a memory access may immediately occur without the need for an operation signaling the location where the address of the location L is stored. According to the invention, the memory access is based on a command from the CPU 22. In one preferred embodiment, a memory access results from the assertion of either the WE# signal or the RE# signal *while the AE# signal is de-asserted.* Preferably, a memory access is based entirely on such a command. For example, referring to Figures 6 and 9, a write data cycle 3 may occur immediately subsequent to the address cycle 2. Alternatively, referring to Figures 6 and 10, a read data cycle 3' may occur immediately subsequent to the address cycle 2." (emphasis added.)[10]

Claims 38-39

Claims 33-39 depend from claim 37. Claims 33-39 are not anticipated for the same reason that the independent claim 37 is not anticipated.

Claims 34 and 40

Amended claims 34 and 40 include the step:

> "(b) receiving a memory access command that does not specify said registers;"

The Wollan reference fails to disclose such a step.

In the rejection of claims 34 and 40, the Examiner cites col. 14, lines 46-65. The cited text is discussed above with reference to claim 37. As mentioned, Wollan teaches a data transfer instruction that includes *selecting* a register pair. Accordingly, Wollan teaches fails to teach the step of receiving a memory access command that does not specify the claimed at least two registers. Therefore, the Wollan reference fails to disclose each and every element of independent claims 34 and 40.

[10] Page 12, lines 5-20.

Claims 35-36 and 41-42

Claims 35-36 depend from claim 34. Claims 41-42 depend from claim 40. Claims 35-36 and 41-42 are not anticipated for the same reason that the independent claims 34 and 40 are not anticipated.

Conclusion

The Wollan reference fails to disclose each and every element of any of the claims. Therefore, Wollan does not anticipate any of the claims. Accordingly, claims 1-42 are in condition for allowance. Applicant respectfully requests that claims 1-42 be allowed, and this application be passed to issue.

Respectfully submitted,

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